AMENDMENTS TO THE CLAIMS

1. (currently amended) An image array pixel comprising:

a charge ~~sharing~~ storing node;

a photosensor coupled to said charge storing node;

a controllable voltage source for supplying one of a first and second voltage level; said first voltage level being higher than said second voltage level;

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being ~~switchably~~ coupled to an output of said controllable voltage source ~~first and second voltage sources for providing first and second voltages, respectively,~~ the other of said source/drain regions being coupled to said charge storing node;

a reset control circuit coupled to a gate of said reset transistor, said reset control circuit for selectively providing a first reset control signal at a first level and a second reset control signal at a second level, said first level being higher than said second level,

said reset control circuit and controllable voltage source being controllable during first, second, and third time intervals such that:

during said second time interval, said reset transistor control circuit supplies said second reset control signal to said gate of said reset transistor while said controllable voltage source provides said second

voltage ~~to operate said reset transistor~~ to partially remove charges from said photosensor,

during said third time interval, said reset transistor control supplies said first reset control signal to said gate of said reset transistor, said controllable voltage source provides said first voltage to substantially remove all charges from said photosensor.

~~a row select transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to the first and second voltages, the gate of said row select transistor being coupled to a third voltage source, said third voltage source being different from said first and second voltage sources, wherein the gate of said reset transistor is coupled to a fourth voltage source being different from said first, second, and third voltage sources.~~

2. (currently amended) The pixel of claim 1, ~~wherein said first voltage is higher than said second voltage~~ wherein said reset control circuit and controllable voltage source are further controllable such that:

during said first time interval, said reset control circuit supplies said first reset control signal to said gate of said reset transistor while said controllable voltage source provides said second voltage to operate said reset transistor to store charges at said photosensor.

3. (currently amended) The pixel of claim [[2]] 1, wherein said second voltage is a ground potential.

4. (cancelled)

5. (Original) The pixel of claim 1, wherein said pixel does not receive any light.

6. (cancelled)

7. (cancelled)

8. (cancelled)

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (cancelled)

15. (cancelled)

16. (cancelled)

17. (cancelled)

18. (Withdrawn) An image array comprising:

a pixel cell;

a power supply circuit for selectively providing a first and second reset voltage; and

a switch circuit for coupling said power supply circuit to a storage node of said pixel cell.

19. (Withdrawn) The image array of claim 18, wherein said power supply circuit comprises:

a first transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first voltage, the other of said source/drain regions being coupled to said storage node; and

a second transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a second voltage, the other of said source/drain regions being coupled to said storage node.

20. (Withdrawn) The image array of claim 19, wherein said only one of said first and second transistors of said power supply circuit is conductive at the same time.

21. (Withdrawn) The image array of claim 20, wherein said first voltage is substantially equal to an operating voltage of a pixel array.

22. (Withdrawn) The image array of claim 20, wherein said second voltage is a lower voltage than said first voltage.

23. (Withdrawn) The image array of claim 22, wherein said second voltage is a ground potential.

24. (Withdrawn) The image array of claim 19, wherein said switch circuit comprises:

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to said output of said power supply circuit, the other of said source/drain regions being coupled to said storage a node.

25. (Withdrawn) The image array of claim 24, further comprising:

a reset control circuit for controlling said reset transistor in said pixel cell, said reset control circuit coupled to said gate of said reset transistor.

26. (Withdrawn) The image array of claim 25, wherein said reset control circuit provides a first and second reset control signal.

27. (Withdrawn) The image array of claim 26, wherein said first control signal is a full reset control signal.

28. (Withdrawn) The image array of claim 27, wherein said second control signal is an intermediate reset control signal.

29. (Withdrawn) The image array of claim 19, wherein first pixel cell is a light opaque pixel cell.

30. (Withdrawn) The image array of claim 19, wherein first pixel cell is disposed in a redundant area of said array.

31. (Withdrawn) The image array of claim 25, wherein said power supply circuit is mutually coupled to a second pixel cell.

32. (Withdrawn) The image array of claim 31, wherein second pixel cell is disposed in a same row of said image array as said first pixel cell.

33. (Withdrawn) A method of operating pixel of pixel array, said method comprising:

flooding a pixel in said array to clear any stored signal;

applying a first reset voltage to said charge storage area of said pixel;

sampling a first voltage signal from said charge storage area;

applying a second reset voltage to said charge storage area;

sampling a second voltage signal from said charge storage area; and

determining a difference between said first and second sampled voltage signals.

34. (Withdrawn) The method of claim 33, wherein said first reset voltage is an intermediate reset voltage, which is less than a fill reset voltage.

35. (Withdrawn) The method of claim 34, wherein said second reset voltage said full reset voltage.

36. (Withdrawn) The method of claim 33, wherein said first reset voltage is a higher voltage than said second reset voltage.

37. (Withdrawn) The method of claim 36, wherein said determining further comprises:

determining said difference in a differential amplifier.

38. (Withdrawn) The method of claim 37, further comprising: converting said difference into a digital form.

39. (Withdrawn) A method of determining the intermediate reset voltage of an image array, said method comprising:

sampling and storing a first set of integrated signals from an array of pixels;

applying a first reset voltage to said array of pixels;

sampling and storing a first set of reset signals from said array of pixels;

applying a second reset voltage to said array of pixels;

sampling and storing a second set of integrated signals from said array of pixels;

applying said first reset voltage to said array of pixels;

sampling and storing a second set of reset signals from said array of pixels; and

determining a difference between said first set and second set of sampled voltage signals.

40. (Withdrawn) The method of claim 39, wherein said first reset voltage is a full reset voltage.

41. (Withdrawn) The method of claim 40, wherein said second reset voltage is an intermediate reset voltage.

42. (Withdrawn) The method of claim 39, wherein said first reset voltage is a higher voltage than said second reset voltage.

43. (Withdrawn) The method of claim 39, wherein said determining step comprises: determining a difference between said first set of integrated and reset sampled and stored voltage signals in a differential amplifier to provide a set of difference signals.

44. (Withdrawn) The method of claim 43, wherein said determining step further comprises: determining a difference between said second set of integrated and reset sampled and stored voltage signals in a differential amplifier to provide a second set of difference signals.

45. (Withdrawn) The method of claim 44, wherein said determining step further comprises: converting said first set of difference signals into a set of digital values.

46. (Withdrawn) The method of claim 45, wherein said determining step further comprises: converting said second set of difference signals into a second set of digital values.

47. (Withdrawn) The method of claim 46, wherein said determining step further comprises: comparing said first and second sets of digital values.

48. (Withdrawn) The method of claim 47, wherein said comparing step comprises: offsetting said first set of digital values by said second set of digital values.

49. (Withdrawn) The method of claim 46, wherein said determining step further comprises: identifying saturated pixels from said first set of digital values.

50. (Withdrawn) The method of claim 49, further comprising: offsetting said first set of digital values corresponding to said saturated pixels by said second set of digital values corresponding to said saturated pixels.

51. (Withdrawn) The method of claim 50, wherein said applying said second reset voltage occurs shortly before said sampling and storing said second set of integrated signals.

52. (cancelled)

53. (cancelled)

54. (cancelled)

55. (cancelled)

56. (Withdrawn) A processor system, comprising:

a processor; an imager array coupled to said processor, one pixel of said imager array comprising: a pixel cell;

a power supply circuit for reflectively providing a first and second reset voltage; and

a switch circuit for coupling said power supply circuit to a storage node of said pixel cell.

57. (Withdrawn) The processor system of claim 56, wherein said power supply circuit further comprises:

a first transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first voltage, the other of said source/drain regions being coupled to said storage node; and

a second transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a second voltage, the other of said source/drain regions being coupled to said storage node.

58. (Withdrawn) The processor system of claim 57, wherein said only one of said first and second transistors of said power supply circuit is conductive at the same time.

59. (Withdrawn) The processor system of claim 58, wherein said first voltage is substantially equal to an operating voltage of a pixel array.

60. (Withdrawn) The processor system of claim 58, wherein said second voltage is a lower voltage than said first voltage.

61. (Withdrawn) The processor system of claim 60, wherein said second voltage is a ground potential.

62. (Withdrawn) The processor system of claim 57, wherein said switching circuit comprises:

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to said output of said power supply circuit, the other of said source/drain regions being coupled to said storage node.

63. (Withdrawn) The processor system of claim 62, further comprising: a reset control circuit for controlling said reset transistor in said pixel cell, said reset control circuit coupled to said gate of said reset transistor.

64. (Withdrawn) The processor system of claim 63, wherein said reset control circuit provides a first and second reset control signal.

65. (Withdrawn) The processor system of claim 64, wherein said first control signal is a full reset control signal.

66. (Withdrawn) The processor system of claim 58, wherein said second control signal is an intermediate reset control signal.

67. (Currently amended) An imaging device, comprising:

a processor;

an imager array coupled to said processor, one pixel of said image array comprising:

a charge sharing node;

a reset control circuit configured to provide a plurality of voltages;

a row select transistor being switchably coupled to a first and second voltage, a gate of said row select transistor being coupled to a row select control line; and

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to [[a]] said first and second voltage, the other of said source/drain regions being coupled to said node, a gate of reset transistor being coupled to a reset control ~~line~~ circuit.

68. (Original) The imaging device of claim 67, wherein said first voltage is higher than said second voltage.

69. (Original) The imaging device of claim 68, wherein said second voltage is a ground potential.

70. (Original) The imaging device of claim 67, wherein said one of said source/drain regions is coupled to only one of said first and second voltages at a time.

71. (new) An imager circuit comprising:

a controllable voltage source for selectively supplying one of a first lower voltage level and a second higher voltage level to a voltage supply line;

a charge storage node;

a photosensor coupled to said storage node;

a reset transistor coupled between said voltage supply line and said storage node, said reset transistor having a gate input; and

a control circuit for providing control signals to said controlled voltage source and gate of said reset transistor, said control circuit configured such that:

during a first time period, said reset transistor is supplied with a gate control signal at a first level while said controllable voltage source supplies said second voltage level to said voltage supply line,

during a second time period, said reset transistor is supplied with a gate control signal at a second level lower than said first level but above a threshold voltage of said reset transistor while said controllable voltage source supplies said second voltage level to said voltage supply line.

72. (new) The imager circuit of claim 71, where said control circuit further configured such that:

during a third time period, said reset transistor is supplied with a gate control signal at a third level being substantially logic level zero to deactivate said reset transistor.

73. (new) The imager circuit of claim 72, where said control circuit further configured such that:

during a fourth time period, said reset transistor is supplied with a gate control signal at said first level while said controllable voltage source supplies said first voltage level to said voltage supply line.

74. (new) The imager of claim 73, further comprising:

a sample and hold circuit selectively coupled to said pixel being controllable such that during a time interval between said first time period and said second time period, said sample and hold is coupled to said charge storage node to store a first stored value,

said sample and hold circuit being controllable such that during a time interval after said second time period, said sample and hold is coupled to said charge storage node to store a second stored value.

75. (new) A pixel array comprising:

at least one pixel circuit comprising:

a storage node for storing charges;

a reset transistor for controlling the charges stored at said storage node;

a circuit for operating said reset transistor to fill the storage node with electrons, to partially remove electrons from said storage node, and to substantially remove all charges from said storage node; and

a readout circuit for providing a first signal representing charges at said storage node after electrons are partially removed from said storage node and a second signal representing charges at said storage node after all charges are removed from said storage node.

76. (new) The pixel array of claim 75 further comprising:

a comparison circuit coupled to said readout circuit for comparing said first signal with said second signal to determine a knee point response characteristic of said pixel circuit.

77. (new) The pixel array of claim 76 wherein said comparison circuit further comprises:

an analog-to-digital converter coupled to said readout circuit.

78. (new) The pixel array of claim 77 wherein said comparison circuit further comprises a differential amplifier circuit, wherein said comparison circuit compares said first signal with said second signal by having said first and second signals being first and second inputs to said differential amplifier circuit.

79. (new) The pixel array of claim 78 wherein said comparison circuit comparison compares said first signal with said second signal after said first and second signals are processed by said analog-to-digital converter.

80. (new) A pixel comprising:

a first voltage source having an output switchable between a first and second reset supply voltage in response to a first control signal;

a charge storage region;

a reset transistor connected between said first voltage source and said charge storage region; and

a control circuit for providing a gate control voltage to a gate of said reset transistor, said control circuit selectively providing a first operating control voltage and a second operating control voltage to said reset transistor, said second operating control voltage being less than said first operating control voltage.

81. (new) The pixel of claim 80, wherein said first voltage source and said control circuit are configured to operate said reset transistor such that a first reset voltage is provided at said storage node when said first reset supply voltage at said second operating control voltage is are provided to said reset transistor and

a second reset voltage is provided at said storage node when said first supply voltage and said first operating control voltage are provided to said reset transistor.

82. (new) The pixel of claim 81, wherein said first voltage source and said control circuit are configured to operate said reset transistor such that said storage region has a third voltage when said second reset supply voltage and said first operating control voltage are supplied to said reset transistor.

83. (new) The pixel of claim 2, further comprising

a differential amplifier configured to provide correlated double sampling of a first signal read from said charge storing node after said

second time interval and a second signal read from said charge storing node after said third time interval.

84. (new) An image array pixel comprising:

a charge storing node;

a photosensor coupled to said charge storing node;

a voltage source;

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being coupled to an output of said voltage source the other of said source/drain regions being coupled to said charge storing node;

a sample and hold circuit having first and second storage areas selectively coupled to said charge storing node; and

a control circuit for operating said reset transistor and said sample and hold circuit for providing a correlated double sampling and holding of a charge integrated signal and a full reset signal during a one sample and hold period and for providing a sampling and holding of a first full reset signal with said reset transistor receiving a first gate control signal and a second less than full reset signal with said reset transistor receiving a second gate control signal which is lower than said first gate control signal during a second sample and hold period.

85. (new) The pixel of claim 84,wherein said pixel being controllable during first, second, third, fourth, and fifth time intervals such that:

during said first time interval, reading out a signal from said charge storing node and storing it in said first storage area of said sample and hold circuit;

during said second time interval, sampling and holding a signal in said second storage area of said sample and hold circuit from said charge storing node after a first full reset signal with said reset transistor receiving said first gate control signal;

during said third time interval, said reset transistor receiving a second gate control signal;

during said fourth time interval, reading out a signal from said charge storing node and storing it in said first storage area of said sample and hold circuit;

during said fifth time interval, sampling and holding a signal in said second storage area of said sample and hold circuit from said charge storing node after a first full reset signal with said reset transistor receiving said first gate control signal.

86. (new) The pixel of claim 84, wherein said third time interval occurs close in time to said fourth time interval.